REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

Claim 1 has been amended to further emphasize that at least one video signal line is between the switches and the display area. This was recited in the original claims and was the basis for traversing the rejection, and yet has apparently been completely overlooked by the Examiner. In addition, **claims 9-16 have been added** to specifically recite three video signal lines, and that the third video signal line is between the switch units and the active area, as shown for example in Fig. 2a as originally filed. None of the amendments constitutes "new matter."

The rejection of claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Kabuto et al (5,151,689) is again respectfully traversed on the grounds that the Kabuto patent does not disclose or suggest **placing the switches *BETWEEN* video signal lines**. According to the Examiner:

> *Applicant argues that Kabuto et al does not teach a driving circuit comprising wherein each of the plurality of switch units is connected to at least one signal line to receive a video signal and is connected to the buffer unit to receive the scanning signal inverted by the buffer* unit.

Somehow, in paraphrasing and responding Applicant's argument, the Examiner has omitted or ignored the limitation that the switch units are located "***between said plurality of video signal lines***," which was emphasized repeatedly both in

Applicant's arguments and in the specification.

If the Examiner will review Figs. 1, 2a, and 3a of the present application, he will notice that, whereas Fig. 1 shows three signal lines 121-123 above the switches 111-113, Fig. 2a shows that switches 221-223 are ***between*** signal lines 212 and 213, and Fig. 3a shows switches that are between signal lines 313 and 311. This difference can be understood from the following graphic.

FIG. 1

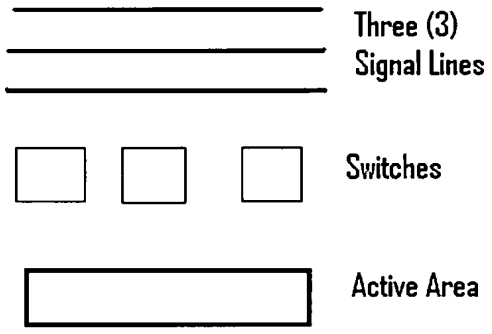
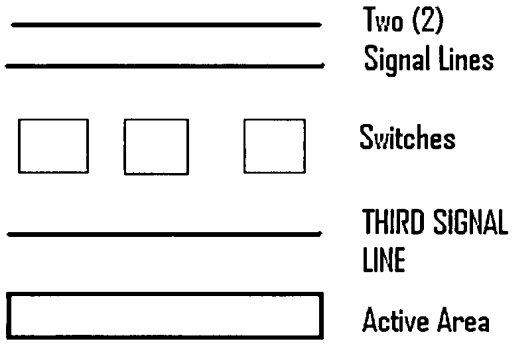


FIG. 2A & CLAIMS



The Examiner will notice that, in Fig. 1 of the present application, which is similar to the arrangement of the Kabuto patent as discussed below, the switches are not between any two signal lines. In Fig. 2A, the switches are ***between*** two of the signal lines, as claimed. Of course, the claimed invention could have one signal line between the switches and active area or two signal lines (see Fig. 3a), so long as the switches are ***between*** the signal lines.

The **placement of the switches *between* signal lines** is **not merely a matter of design choice**, but rather addresses a serious problem in the prior art, namely the problem of parasitic capacitance between signal lines and inverter connections. The reason for moving at least one of the signal lines is, as explained in the introduction to the present application and in the previous response, is to eliminate parasitic capacitances by **reducing the number of cross-over points** between the inverter circuit and the signal lines.

It is respectfully submitted that it is not proper to ignore claim limitations as the Examiner has done in ignoring the recitation that the switches are between signal lines, and the arguments made in the previous response concerning the location of the switches. According to MPEP 707.07(d), the Examiner should consider each claim limitation and not just those found in the reference while ignoring those not found in the reference. Furthermore, although the original claims clearly distinguish the Kabuto patent, the claims have nevertheless been amended to further emphasize the placement of the signal lines, by reciting that at least one signal line is between the switches and the display area, as shown in Figs. 3a and 3b. This is essentially the same as the original recitation of the switches being between signal lines but even more clearly points out the location of the signal lines on each side of the switches.

In none of the embodiments disclosed by Kabuto are the switches M11, M12, . . . controlled by the scanning (inverter) signal lines Ga1, Ga2, . . . situated between video signal lines Dr1, Dr2, ... Instead, switches M11, M12, . . .are located adjacent the active areas in the display matrix. The switches of Kabuto are not *between* signal lines, as claimed, and there are no signal lines *between* the switches and the active areas of the display matrix.

To the contrary, Kabuto actually places the switches M11, M12, . . . *in* the active matrix.

In order to understand the relationship between the circuit disclosed by Kabuto and the claimed invention, it is important to understand the relationship between the claimed buffer unit for inverting a scanning signal. In the claimed invention, the switch units are connected to receive video signals from the video signal line and to output the video signals in response to scan signals from the buffer unit or inverters. In Kabuto, the scan lines are Ga1, Ga2, . . . and the video lines are Dr1, Dr2, . . ., while the switches are M11, M12, . . ., which are controlled by the scan lines to supply signals from the video lines to the light emitting areas E11, E12, ... The active area is therefore the area to the right of driving circuit 4 in Fig. 1, which is shown in detail in Fig. 15. As shown therein, the scanning lines (Ga1, Ga2, ...Ga9) are provided for pixels in one row and the signal lines (Dr1, Dr2, ...) are arranged at intervals of each pixel. A display area, not a circuit area, as shown in Fig 15, is composed by several pixels as is well known in the technical field. **Consequently, it can be seen that the switches of Kabuto are actually located *in* the active area, and there are clearly no video signal lines between the switches and the active area as claimed, and that the switches are not located between video signal lines as also claimed**.

It is noted that, according to Fig. 16 of Kabuto, the shift register 21 is connected to gate circuits or selectors 22 and then the gate circuits or selectors 22 are connected a switch 23 and an output buffer 24. The output buffer 24 amplifies the image signals and then outputs the image signals to pixels rather than inverting a scanning signal. Hence, the function of the output buffer 24 is different from that of the buffer unit in the present application, and the circuit of Kabuto does not

operate in the same manner as the claimed invention. Since Kabuto does not disclose a circuit that operates the same manner as the claimed invention, one of ordinary skill in the art could not possibly have modified the circuit of Kabuto to have the *structure* of the claimed invention, namely switches ***between*** signal lines and signal lines ***between*** the active area and the switches.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the application are now believed to be in order, and such action is hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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